A Novel Balanced Ternary Adder Using Recharged Semi-Floating Gate Devices

Henning Gundersen and Yngvar Berg

Department of Informatics, Microelectronic Systems Group, University of Oslo

Blindern, NO-0316, Oslo, Norway

Email: henningg@ifi.uio.no

Abstract—This paper presents a novel voltage mode Balanced Ternary Adder (BTA), implemented with Recharged Semi-Floating Gate Devices. By using balanced ternary notation, it is possible to take advantage of carry free addition, which is exploited in designing a fast adder cell. The circuit operates at 1 GHz clock frequency. The supply voltage is only 1.0 Volt. The circuit is simulated by using Cadence®Analog Design Environment, with CMOS090 process parameters, a 90nm General Purpose Bulk CMOS Process from STMicroelectronics with 7 metal layers. All the capacitors are metal plate capacitors, based on vertical coupling capacitance between stacked metal plates.

I. INTRODUCTION

Humans count by tens, machines count by twos, this sums up the way we do arithmetic today. However, there are countless other ways to count. This paper will present a ternary adder which uses base 3 representation. 'Ternary numbering systems is the most efficient of all integer bases' as Brian Hayes claims in his article *Third Base*[1]. Ternary number systems use number representation with radix=3, compared with binary, which uses radix=2. Another way of representing a ternary number is by using a balanced ternary notation. 'Perhaps the prettiest number system of all' as Donald Knuth said in his book, *The Art of Computer Programming* [2]. In the balanced ternary the digits are also powers of 3, as in ordinary ternary numbers, but they are 'balanced' since they are symmetrical about zero. Another approach by using ternary logic in fast adder design, is presented by Rajashekhara et.al. [3]

A given example of a balanced ternary number is the decimal number 23. It is written in balanced ternary notation as: $10\bar{1}\bar{1}$. This numeral is interpreted as: $1x3^3 + 0x3^2 - 1x3^1 - 1x3^0$, or $27 + 0 - 3 - 1$, in decimal notation. The balanced ternary number system has also some nice properties:

- Negation is easy, change $\bar{1}$ with 1, and vice versa. If we use the example -23, the result will be $\bar{1}011$ in balanced ternary notation.
- The sign of a number is given by its most significant nonzero 'trit'¹
- The operation of rounding to the nearest integer is identical to truncation.

¹One trit has 3 values, the values are (-1, 0, 1), it is analogous to bit in the binary world (0, 1).

d) Addition and subtraction are essentially the same operation: just negate one number, and afterwards do an adding operation.

The multiple-input Floating-Gate (FG) transistors can be used to simplify the design of multiple-valued logic [4]. The initial charge on the floating-gates may vary significantly and therefore impose a very severe inaccuracy, unless we do apply some form of initialization. Research on floating-gate reset strategies have been presented by Kotani et.al. [5], and by Berg et.al. [6].

Floating-Gate (FG) circuits need to be initialized, either once initially or frequently. The once and for all initialization is synonymous with programming. By recharging the FG frequently we avoid problems with any leakage currents and random or undesired disturbance of the floating-gate charges, and we convert the non-volatile floating gates to Semi Floating-Gates (SFG)[6]. The reset or recharged scheme may be used to overcome some problems associated with the floating-gate circuit design. The recharged condition is different than the reset in clocked-Neuron-MOS logic proposed by Kotani et.al. [5].

When resetting or recharging a gate the inputs are recharged simultaneously and are not set to a reference voltage. While recharging, the gates are short-circuited using a local recharge switch (+Clk), the output and the semi floating-gate on the input is forced to $V_{dd}/2$, see figure 1.

The recharged scheme is similar to biasing of single-ended auto-zeroing comparators, which have been used in high-speed flash AD converters. The main purpose of the recharged scheme is to initialize or recharge the semi-floating-gates to an equilibrium state which can be utilized to yield fast binary and multiple-valued signal processing. In addition we may reduce the effect of mismatches, especially transistor mismatches, and power supply noise. The recharged scheme provides a simple, fast and accurate recharge to the equilibrium state for all gates regardless of logical depth. We use the term Recharged Logic (RL) or Recharged Semi-Floating Gate Logic (RSFGL) for the circuits presented in this paper [7]. The SFG circuits are recharged to the initial equilibrium state, namely $V_{dd}/2$.

This paper will present a novel carry free Balanced Ternary Adder (BTA) using Recharged Semi-Floating Gate (RSFG) devices. The truth table of the presented adder is shown in table I. Section II will briefly cover some of the building blocks used in Recharged Semi-Floating Gate design. In section III we will look closer to the realization of the voltage mode Balanced Ternary Adder (BTA).

TABLE I
THE TRUTH TABLE OF THE BALANCED TERNARY ADDER

X	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1
Y	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1
SUM	$\bar{1}1$	$0\bar{1}$	00	$0\bar{1}$	00	01	00	01	$1\bar{1}$

II. FUNDAMENTAL BUILDING BLOCKS USED IN RECHARGED SEMI-FLOATING GATE (RSFG) DESIGN

A. The Recharged Semi-Floating Gate (RSFG) Inverter

Fig. 1. Schematic diagram of a Recharged Semi-Floating Gate Inverter. The transistor sizes are P_e ($w = 460nm$ and $l = 100nm$) and N_e ($w = 120nm$ and $l = 100nm$)

A Recharged Semi-Floating Gate (RSFG) inverter is shown in figure 1. The RSFG inverter act just like an ordinary inverter, except that it has a local feedback switch (+Clk) connected between the input gates and the output. By equalizing the β s we obtain an equilibrium state when the recharged signal is 1, and the output and the gate are driven towards $V_{dd}/2$. The recharge frequency is twice the frequency of the input signal.

B. The Recharged Semi-Floating Gate (RSFG) Ternary Inverter

The Recharge Semi-Floating Gate (RSFG) MVL-Inverter [8] in figure 2 is an important application. This is a key element in Multi-Valued Logic [6]. A MVL inverter, also called an analog inverter, is an inverter with a negative feedback mechanism, C_f [9]. The voltage gain of this circuit is $A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = -1$. The transfer characteristic of the analog inverter is given by equation 1.

$$V_{out} = V_{dd} - V_{in} \quad (1)$$

A MVL inverter can be used to generate the NOT or the Negation function in ternary logic. A truth table of a Ternary NOT function is shown in table II.

Fig. 2. Schematic diagram of the Recharged Semi-Floating Gate MVL Inverter, which generates the Ternary NOT function. The transistor sizes are P_e ($w = 460nm$ and $l = 100nm$) and N_e ($w = 120nm$ and $l = 100nm$)

TABLE II
THE TRUTH TABLE OF THE TERNARY NOT FUNCTION

In	Out
$\bar{1}$	1
0	0
1	$\bar{1}$

C. The Auto-Zero Circuit (AZC)

The input stages needs an Auto-Zero Circuit (AZC) as shown in figure 3. An Auto-Zero circuit can be seen as a signal converter which converts an input signal to a valid recharge signal [10]. The recharge frequency is twice the frequency of the input signal. The AZC has two Pass-Gate Circuits, clocked

Fig. 3. Schematic diagram of the Auto-Zero circuit The transistor sizes are P_e ($w = 130nm$ and $l = 100nm$) and N_e ($w = 130nm$ and $l = 100nm$)

with the opposite clock phase. The upper Pass-Gate Circuit in figure 3 has $V_{dd}/2$ as the input, and the lower Pass-Gate has V_{in} as input. The output signal V_{out} will then have the signal level of $V_{dd}/2$, in the recharge period, which is set by the upper Pass-Gate circuit, and V_{in} in the precharged period. The X and Y signals shown in figure 5 are examples of Auto-Zeroed input signals.

Fig. 4. Schematic diagram of the Balanced Ternary Adder ($C1, C2, C3, C4, C5, C6, C7, C8, C11, C12, C13, C16, C17, C20, C21 = 1fF, C9, C15 = 1.5fF, C10 = 7fF, C14 = 3fF, C18 = 2fF, C19 = 4fF$)

III. THE BALANCED TERNARY ADDER

A Balanced Ternary Adder (BTA) takes two Ternary inputs (X and Y) and generate the SUM output (S0 and S1), and it offers carry free addition. The truth table of the BTA is shown in table I. The complete schematic diagram of the Balanced Ternary Adder circuit is shown in figure 4.

A. The Pre-Adder stage

The Pre-Adder stage is a simple adder. The Pre-Adder adds the two input signals X and Y electrically, using a two-input MVL inverter. The Pre-Adder stage consists of capacitors C7, C8, C9, C10, C11 and Inverter i3 and i6. Inverter i3 is a two inputs MVL inverter. Input signal X is connected to C7 and the Y signal is connected to C8. The two input signals will be added together and inverted. The output signal from i3 has to be amplified and inverted. This is done by the ternary inverter i6, the ternary output signal from the Pre-Adder stage is shown in figure 5. The output signal of the Pre-Adder is not correct. When both X and Y is high (1) or when both X and Y are low ($\bar{1}$), the signal has to be inverted to generate a correct SUM 0 signal which correspond to the truth table I.

B. The Carry detect stage

The Carry detect stage will either detect when both X and Y is high or both X and Y is low. Furthermore this will generate a Binary high- or low-Carry signal. The Carry detect stage consists of C1, C2, C3, C4, C5, C6 and four inverters i1, i2, i4 and i5. The main idea is to use the threshold elements i1 and i2, a three input FG inverter, to detect the carry signal. To detect carry high, the three input FG inverter i1 is used. The Auto-Zeroed X is connected to C3, Auto-Zeroed Y is

connected to C2. C1 is connected to a Auto-Zeroed *gnd* signal. If both X and Y is high, the inverter i1 will set the output Low, else the output will be determined by the Auto-Zeroed *gnd* signal, and the output of i1 will be set high. The output will only be set low if both X and Y is High. The logic levels of X and Y, if they are high is $= 900mV$. The *gnd* signal is 0 V. Since all of the inputs have the same weight, ($C1=C2=C3$) hence it will be set low only when both X and Y are 1. Carry low detection is done in the same manner, except if both X and Y are low, the output of inverter i2 is set high, else the output is set low. As figure 4 shows C4 is connected to the Auto-Zeroed V_{dd} and all of the input capacitors has the same weight ($C4=C5=C6$). The logic levels of X and Y low ($\bar{1}$) are $100mV$ and $V_{dd} = 1.0V$, hence both X and Y have to be low to set inverter i2 high. Inverter i4 and i5 equalize and inverts the signal, the output of the Carry detect stage, C-LOW and C-HIGH is shown in figure 5. Inverter i7 is a binary to ternary converter. It makes a summation of C-LOW and C-HIGH. The output signal SUM-CARRY in figure 5 is a ternary representation of the Carry signals.

C. The output stages

1) *SUM 1*: To generate the SUM 1 signal we only need a ternary inversion of the SUM-CARRY signal, this is done by the ternary inverter i9.

2) *SUM 0*: To generate SUM 0 we need to invert the PRE-ADDER output signal either when both X and Y are low or high at the same time. This is achieved by the two input MVL inverter i8. C14 has to be twice the value of C15 to achieve this. The output of i8 is the inverted SUM 0 signal, this is why the output has to be inverted in inverter i10, which generate

Fig. 5. Simulation results for the Balanced Ternary Adder shown in figure 4.

the correct SUM 0 signal shown in figure 5. Furthermore this correspond with the truth table I. Figure 6 shows an example of a two trits adder, using the Balanced Ternary Adder blocks.

D. The subtraction circuit

To make a balanced Ternary Subtraction Circuit either X or Y need to be inverted as shown in figure 7. Y is inverted using the RSFG Ternary Inverter shown in figure 2. This application generates the balanced ternary subtraction, $X - Y$.

IV. CONCLUSIONS

In this paper a novel Balanced Ternary Adder (BTA) has been presented. A subtraction circuit using the BTA, can easily be made by a ternary inversion of one of the input signals. It offers carry free addition, and this adder can be used as a building block in designing a fast multiplier circuit. It operates at a clock frequency at 1 GHz. The supply voltage is only 1.0 Volt.

Fig. 6. An example of a 2 trits Balanced Ternary Adder

Fig. 7. A Balanced Ternary Subtractor Circuit

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