Fast Addition Using Balanced Ternary Counters Designed With CMOS Semi-Floating Gate Devices

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Abstract

This paper presents ternary counters using balanced ternary notation. The balanced ternary counters can replace binary full adders or counters in fast adder structures. The circuits use recharged CMOS semi-floating gate (RSFG) devices. By using balanced ternary notation, it is possible to build balanced ternary addition circuits, which can add both negative and positive operands, by using the same adder blocks. The circuit operates at a clock frequency of 1 Ghz. The supply voltage 1.0 Volt.

1 Introduction

Nowadays nearly all addition done in an arithmetic unit (ALU) in a modern computer, uses binary operands. By using ternary notation we can take advantage of the possibilities lying in the ternary numbering system. If we are using balanced ternary numbers, also called Signed-Digit Numbers [12], we can add both negative and positive numbers without any use of a sign bit. The so-called 'Brousentsov's Ternary Principle' of computer design was initially realized in the Setun computer [14] and this computer was based on the 'ternary-symmetrical number system', which is another name for the balanced ternary notation.

As early as 1840 Thomas Fowler, a self-taught English mathematician, invented a ternary mechanical calculating machine which used balanced ternary notation. All details on the calculating machine was lost, until recently. A research project, started in 1997, have managed to get the information which was needed to create a complete historical replica [4]. Fowler used the terms -, 0 and + for a negative, a zero and a positive number. In this paper the terms $\bar{1}$, 0 and 1 will be used.

There has been several attempts to implement arithmetic applications by using the ternary numbering system, but they lack commercial success [8] [3].

1.1 The Balanced Ternary Numbering System

Brian Hayes claims in his article *Third Base* [7] 'Ternary numbering systems are the most efficient of all integer bases'. In the balanced ternary notation the digits are also powers of 3, as they are in ordinary ternary numbering systems. However they are 'balanced' since they are symmetrical about zero. Balanced ternary notation is 'Perhaps the prettiest number system of all' as Donald Knuth says in his book, *The Art of Computer Programming* [10].

A balanced ternary number $10\bar{1}\bar{1}$ (23_{10}), is interpreted as: $1x3^3 + 0x3^2 - 1x3^1 - 1x3^0$, or $27 + 0 - 3 - 1$, in decimal notation.

The balanced ternary number system has some advantageous properties:

- 'Ternary inversion' [14] is easy, change $\bar{1}$ with 1, and vice versa. If we use the example -23, the result will be $\bar{1}011$ in balanced ternary notation.
- The sign of a number is given by its most significant nonzero 'trit'¹.
- The operation of rounding to the nearest integer is identical to truncation.
- Addition and subtraction are essentially the same operation: just apply the rules of 'ternary inversion' to one of the operands, and afterwards do an adding operation.

The truth table of the rule of 'ternary inversion' is shown in table 1.

Table 1. The rule of 'ternary inversion'

x	$\bar{1}$	0	1
$\bar{x}$	1	0	$\bar{1}$

¹One trit has 3 values ($\bar{1}$, 0, 1), it is analogous to bit in the binary world (0, 1).

1.2 Balanced Ternary Counters

A balanced ternary counter (BTC) is comparable with a ternary full adder, where the carry signal can have all logic values ($\bar{1}$, 0 and 1)². A balanced ternary adder sums up the inputs X_i , where i is number of trits of the same weight, and gives an output in balanced ternary notation. Truth tables of balanced ternary counters are shown in table 2 and table 4.

A (4,2) counter corresponds to a 4-input ternary full adder, where the carry signal can take all three logic values.

This paper present balanced ternary adder structures, using (3,2) and (4,2) ternary counters, it has also been called 4 to 2 reducers [15]. A (4,2) ternary counter has 4 balanced ternary inputs ($X_1..X_4$) and two balanced ternary outputs (S_0, S_1).

An interesting ternary full adder implemented in Depletion/Enhancement CMOS technology was presented in 1985 [9], but it didn't achieved any commercial success.

Earlier work on this problem was a balanced ternary adder which were presented in Singapore at the ISMVL conference in 2006 [6]. This was a balanced (2,2) ternary adder, it had two balanced ternary inputs (X and Y) and two balanced ternary outputs (S_0, S_1).

Table 2. The truth table of a balanced ternary (4,2) counter

$\sum_{i=1}^4 X_i$	-4	-3	-2	-1	0	1	2	3	4
S_0	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1
S_1	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1

1.3 Recharge Semi-Floating Gate Devices

The multiple-input floating-gate (FG) transistors can be used to simplify the design of multiple-valued logic [13]. The initial charge on the floating-gates may vary significantly and impose a very severe inaccuracy, unless we do apply some form of initialization. Research on floating-gate reset strategies have been presented by Kotani et.al. [11], and by Berg et.al. [1].

Floating-gate (FG) circuits need to be initialized, either once initially or frequently. The once and for all initialization is synonymous with programming. By recharging the FG frequently we avoid problems with any leakage currents and random or undesired disturbance of the floating-gate charges, and it converts the non-volatile floating gates

to semi floating gates (SFG)[1]. The reset or recharge scheme may be used to overcome some problems associated with the floating-gate circuit design. The capacitors in the CMOS recharged SFG design, presented in this paper, are metal plate capacitors based on vertical coupling capacitance between stacked metal plates.

1.3.1 The Recharged Semi-Floating Gate (RSFG) Ternary Inverter

Figure 1. Schematic diagram of the Recharged Semi-Floating Gate MVL Inverter, which generates the Ternary NOT function. (P_e : $w/l = 460nm/100nm$ and N_e : $w/l = 120nm/100nm$)

The Recharge Semi-Floating Gate (RSFG) MVL-Inverter in figure 1 is an essential building block [5]. It is a key element in Multi-Valued Logic [1]. The Clk pulse (+Clk) is given by the recharge frequency, which is twice the frequency of the input signal. The voltage gain of this circuit is $A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{C_i}{C_f} = -1$, if the input capacitor (C_i) is equal to the feedback capacitor (C_f).

The transfer characteristic of an ideal analog inverter is given by equation 1 [2].

$$V_{out} = V_{dd} - V_{in} \quad (1)$$

A MVL inverter can be used to generate the 'ternary inversion', $x = \bar{x}$, as shown in table 1.

2 Implementation of the Balanced Ternary (4,2) Counter

A schematic diagram of the presented balanced ternary (4,2) counter is shown in figure 2. The (4,2) counter is implemented using CMOS recharged semi-floating gate (SFG) devices.

²The logic levels are: $\bar{1} = 100mv$, $0 = 500mv$ and $1 = 900mv$, $V_{dd} = 1V$

Figure 2. A Schematic diagram of the balanced ternary (4,2) counter ($C_1..C_4, C_7..C_{10}, C_{14}..C_{19} = 500.5aF$, $C_5, C_6 = 374.4aF$, $C_{13} = 1.503fF$, $C_{20}, C_{22}, C_{25} = 374.4aF$, $C_{21} = 6.69fF$, $C_{23} = 423.2aF$, $C_{24} = 1.234fF$)

2.1 The Balanced Ternary (4,2) Counter

2.1.1 The Carry Detect Stage

The carry detect stage generates a ternary carry signal, when the input signals $\sum_{i=1}^4 X_i$ is less than -2 and greater than 2 . This is achieved by using a 5 input threshold circuit (i1 and i3). By focusing at figure 2 we can see that the 4 inputs $X_1..X_4$, are compared to the clock pulse '+Clk' and '-Clk', connected respectively to input capacitors C_5 and C_6 .

The upper circuits i1 and i2 generates the binary 'C-HIGH' signal, which is set to the logic level '1' when the sum of the inputs X_i , are greater than 2 . The input capacitors $C_1..C_4$ are equal. Capacitor C_5 determines the threshold of i1, by comparing the $\sum_{i=1}^4 X_i$ with the '+Clk' signal (The '+Clk' signal is in phase with reference clock).

'C-LOW' is set in a similar way, except it will be set to logic level ' $\bar{1}$ ', when the sum of the inputs X_i is less than -2 . The threshold of i3 is determined by the capacitor C_6 , which is connected to the '-Clk' signal (The '-Clk' is in opposite phase with the reference clock).

The inverter i5 is a binary to ternary converter, it converts the two binary carry signals (C-LOW, C-HIGH) to a balanced ternary carry signal ($SUM1$).

2.1.2 The Output Stages, SUM 0 and SUM 1

To generate the correct 'SUM 1' signal, we need to do a ternary inversion of the output signal of inverter i5 ($SUM1$), this is done by using the ternary inverter i6. The adder circuits i7 and i8, generates the 'SUM 0' signal. This is done by weighting the inverted ' $SUM0$ ' three times the input signals X_i , by choosing C_{13} three times larger than each of the input capacitors $C_{14}..C_{17}$ ($C_{13} = 1.50fF$, $C_{14}..C_{17} = 500.5aF$). Figure 3 shows a typical plot of the SUM 0 and SUM 1 signal at a 1 GHz clock frequency. This verifies the logical operation of the BT (4,2) counter circuit shown in table 2.

To make a (3,2) counter, we just need to apply a small modification, we can easily remove three of the input capacitors from the (4,2) counter, as shown in figure 4. Or we can connect one of the inputs of the (4,2) counter to logic level '0' = $V_{dd}/2$.

3 Ternary Applications Using Balanced Ternary Counters

A balanced ternary (13,3) counter can be made by using 5 ternary (4,2) counters, as shown in figure 5. The

Table 4. The truth table of the balanced ternary (13,3) counter

$\sum_{i=1}^{13} X_i$	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13
S_0	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1	$\bar{1}$	0	1
S_1	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	1	1	1
S_3	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Figure 3. Typical outputs from the (4,2) balanced ternary counter shown in figure 2

truth table of the (13,3) counter can be seen in table 4. A block diagram of the complete 4 trits balanced ternary parallel adder using (4,2) BTC's is shown in figure 6. The input vectors are: $X_i = [1\bar{1}10]$, $Y_i = [\bar{1}\bar{1}11]$, $X_i = [0010]$, which correspond with $15-32+3=-14$ in decimal notation. The $SUM = [\bar{1}111]_3 = -14_{10}$. Figure 7 verifies the operation of the circuit. It is also possible to build a Wallace tree structure by using balanced ternary counters. A Wallace tree adder sums up all trits of the same weights in a merged tree, and do not add the partial products in pairs as a balanced ternary parallel adder does. Figure 8 shows a balanced ternary Wallace tree adder.

3.1 Advantages Using Balanced Ternary Counters

Mostly all of the binary adder structures are directly convert able to balanced ternary adder structures. This means you can be able to replace the binary full adders with ternary

Figure 4. A block diagram of a balanced ternary (3,2) counter

balanced counters, and still have the same functionality. However there is an advantage using balanced ternary notation, you do not have to worry about the sign bit, and you need less trits to make the same resolution.

Figure 6 shows a 4-trits parallel balanced ternary adder (BTA), which is comparable with a 6-bit ripple carry adder if we consider the resolution. To build a 6-bit ripple carry adder we need 6 full-adders (FA), compared to 4 balanced ternary counters (BTC). A typical binary FA uses 28 transistors, the presented BTC uses 32 transistors. This gives us, a 4-trits balanced ternary adder needs 128 transistors, compared to a binary 6-bits adder which needs 168 transistors. See table 3. A 11-bit FA uses 308 transistors this is comparable with a 7-trits BTA which uses 224 transistors. Figure 9 shows this graphically, even for low resolutions it is better to use a parallel BTA compared to a binary ripple carry adder. It is also possible to make carry-save adder structures using balanced ternary counters. This makes it easy to implement balanced ternary counters in fast addition structures, based on binary logical adder theory.

A floating gate structure will generally generate a larger chip area compared to a conventional design because of the capacitors. By using very small metal-capacitors and using stacking, we are able to minimize the chip area. The used 90nm CMOS process from STMicroelectronics, has 7 metal layers.

Table 3. Comparison between a binary ripple carry adder and a parallel balanced ternary adder

Bits	Resolution	Transistors	Trits	Resolution	Transistors
1	2	28	1	3	32
2	4	56	2	9	64
3	8	84	3	27	96
4	16	112	4	81	128
5	32	140	5	243	160
6	64	168	6	729	192
7	128	196	7	2187	224
8	256	224	8	6561	256
9	512	252	9	19683	288
10	1024	280	10	59049	320
11	2048	308	11	177147	352
12	4096	336	12	531441	384
13	8192	364	13	1594323	416
14	16384	392	14	4782969	448
15	32768	420	15	14348907	480
16	65536	448	16	43046721	512

4 Conclusions

In this paper, a balanced ternary adder structures using balanced ternary counters has been presented. It has the beneficial properties as following:

1. There is no reason to worry about the sign bit, since the structures use balanced ternary notation.
2. The resolution compared to numbers of transistor gives a higher resolution than with a typical binary solution, this is shown graphically in figure 9.

It is possible to build fast addition structures, using the theory from the binary world. The simulation results shows that the circuits may be able to operate at clock frequency of 1 GHz. The circuits can be made using a conventional CMOS process. We are using a 90nm general purpose bulk CMOS process from STMicroelectronics with 7 metal layers.

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Figure 5. A balanced ternary (13,3) counter

Figure 6. A Block schematic diagram of a 4 trits parallel balanced ternary adder

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Figure 7. Typical output signals ($S0..S4$) of the 4 trits parallel adder shown in figure 6. $SUM = [0\bar{1}111]$. The clock frequency is 1 GHz

Figure 8. A balanced ternary Wallace tree adder, using (3,2) ternary counters

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Figure 9. Resolution compared to number of transistors of the presented parallel balanced ternary adder and a typical binary ripple carry adder