Ultra-Low-Voltage Floating-Gate Transconductance Amplifiers

Yngvar Berg, Tor S. Lande, *Member, IEEE*, Øivind Næss, and Henning Gundersen

Abstract—Ultra-low-voltage (ULV) floating-gate differential amplifiers are presented. In this paper, we present several different approaches to CMOS ULV amplifier design. *Sinh*-shaped and *tanh*-shaped transconductance amplifiers are described. Measured results are provided.

Index Terms—Analog floating-gate circuits, floating gate, low power, low voltage, low-voltage amplifiers.

I. INTRODUCTION

LOOKING into the future, ultralow supply voltage (ULV) ($V_{dd} < 1$ V) is coming. Improved precision in production will permit a reduced threshold voltage with improved matching, but still the threshold voltage will “steal” an increasing part of the available headroom.

The ULV floating-gate analog circuits (FGUVMOS) presented in this paper can operate down to approximately 100 mV in weak inversion. In the following analysis, all transistors are assumed to be in saturation; hence only the saturation voltage and required frequency response limit the minimum usable supply voltage. The threshold shifting required for operating the floating-gate circuits presented in this paper is discussed in [1]–[3].

In Section II, the FGUVMOS transistor and the generic FGUVMOS circuit are presented, and the sinh-shaped and tanh-shaped nonsymmetric ULV amplifiers are presented in Section III, including measured data for the AMS 0.8- μ double-poly process [4]. In Section IV, a compact symmetric ULV sinh-shaped transconductance amplifier is presented, and the symmetric ULV amplifier with tunable transconductance is described in Section V. Measured data for the symmetric ULV circuits in Sections IV and V are relevant for the AMS 0.6- μ double-poly process.

II. FGUVMOS CIRCUITS

The generic FGUVMOS circuit is shown in Fig. 1. For a multiple-input FGUVMOS transistor, each input has by design an effective coupling capacitance C_i to the floating gate. The input signal (*control gate*) is attenuated with a factor $k_i = C_i/C_T$, where C_T is the total load capacitance seen from the gate. k_i is called the capacitive division factor for input i .

Fig. 1. The generic FGUVMOS circuit.

The m -input floating-gate transistor currents are given by

$$I_{ds(nMOS)} = I_{bec} \prod_{i=1}^m \exp \left\{ \frac{1}{nU_t} (V_i - V_{dd}/2) k_i \right\}$$

$$I_{ds(pMOS)} = I_{bec} \prod_{i=1}^m \exp \left\{ \frac{1}{nU_t} (V_{dd}/2 - V_i) k_i \right\}$$

where I_{bec} is the programmed *equilibrium current*. Assuming a pMOS and an nMOS with common control gates and equal capacitive factors, respectively, we have that

$$I_{ds(pMOS)} = \frac{(I_{bec})^2}{I_{ds(nMOS)}}.$$

III. ULTRA-LOW-VOLTAGE FLOATING-GATE AMPLIFIERS

The minimum supply voltage in low-voltage circuits [5] can be defined as $V_{sup, min} = 2(V_{gs} + V_{sat})$. The low-voltage circuits are able to operate on a supply voltage of two stacked gate-source voltages and two saturation voltages. Differential amplifiers are biased with a transistor feeding a differential pair. The current level is set by the bias transistor, and the minimum input voltage in an nMOS input pair is given by $V_{bias} + nV_{dsat} < V_{in} < V_{dd}$, where n is the slope factor modeling the body effect. The bias voltage is proportional to the threshold voltage for a given bias current. To provide a cutoff in the megahertz range, the bias transistor cannot be operated in deep weak inversion. Hence the input voltage and supply voltage are limited by the threshold voltage, the saturation voltage, and the body effect ($V_{in, min}$, $V_{dd} > 1$ V).

By eliminating the bias transistor, we can decrease the supply voltage further (to $n4U_T \approx 200$ mV). The challenge is to de-

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Fig. 2. ULV floating-gate sinh-shaped transconductance amplifier.

sign a differential input stage without the traditional differential pair. The overlap capacitance C_{gd} is added to the Early effect and can be observed as an increased output conductance. By increasing the floating capacitors compared to the inherent MOS capacitors and increasing the transistor length, the output conductance can be reduced to an acceptable value for amplifiers and digital circuits.

A. The SINH Shaped Amplifier

A sinh-shaped transconductance amplifier is shown in Fig. 2. The currents I_1 and I_2 can be expressed as

$$\begin{aligned} I_1 &= I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \exp\left\{\frac{k_1}{nU_T} \left(V_{in1} - \frac{V_{dd}}{2}\right)\right\} \\ &= I_{bec} \exp\left\{\frac{k_4}{nU_T} \left(\frac{V_{dd}}{2} - V_1\right)\right\} \\ I_2 &= I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \exp\left\{\frac{k_1}{nU_T} \left(V_{in2} - \frac{V_{dd}}{2}\right)\right\} \\ &= I_{bec} \exp\left\{\frac{k_4}{nU_T} \left(\frac{V_{dd}}{2} - V_2\right)\right\}. \end{aligned}$$

Assuming that $k_3 = k_4$ and $k_1 = k_2$, I_4 and I_5 become

$$\begin{aligned} I_4 &= I_{bec} \exp\left\{\frac{k_2}{nU_T} \left(\frac{V_{dd}}{2} - V_{in2}\right)\right\} \exp\left\{\frac{k_3}{nU_T} \left(\frac{V_{dd}}{2} - V_1\right)\right\} \\ &= I_1 \exp\left\{\frac{k_2}{nU_T} \left(\frac{V_{dd}}{2} - V_{in2}\right)\right\} \\ &= I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \exp\left\{\frac{k_1}{nU_T} (V_{in1} - V_{in2})\right\} \\ I_5 &= I_{bec} \exp\left\{\frac{k_2}{nU_T} \left(\frac{V_{dd}}{2} - V_{in1}\right)\right\} \exp\left\{\frac{k_3}{nU_T} \left(\frac{V_{dd}}{2} - V_2\right)\right\} \\ &= I_2 \exp\left\{\frac{k_2}{nU_T} \left(\frac{V_{dd}}{2} - V_{in1}\right)\right\} \\ &= I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \exp\left\{\frac{k_1}{nU_T} (V_{in2} - V_{in1})\right\}. \end{aligned}$$

Assuming that $I_6 = I_4$, the output current becomes

$$\begin{aligned} I_{out} &= I_5 - I_6 \\ &= 2I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \\ &\quad \cdot \sinh\left\{\frac{k_1}{nU_T} (V_{in2} - V_{in1})\right\}. \end{aligned}$$

Measured output current of the sinh-shaped transconductance amplifier is shown in Fig. 3.

Fig. 3. Measured output current of the sinh-shaped transconductance amplifier with $V_{dd} = 0.8$ V.

B. The TANH-Shaped Amplifier

A tanh-shaped transconductance amplifier is shown in Fig. 4. The currents I_1 , I_2 , and I_3 can be expressed as

$$\begin{aligned} I_1 &= I_{bec} \exp\left\{\frac{k_3}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \\ &\quad \cdot \exp\left\{\frac{k_1}{nU_T} \left(V_{in1} - \frac{V_{dd}}{2}\right)\right\} \\ I_2 &= I_{bec} \exp\left\{\frac{k_3}{nU_T} \left(V_b - \frac{V_{dd}}{2}\right)\right\} \\ &\quad \cdot \exp\left\{\frac{k_1}{nU_T} \left(V_{in2} - \frac{V_{dd}}{2}\right)\right\} \\ I_3 &= I_{bec} \exp\left\{\frac{k_5}{nU_T} \left(\frac{V_{dd}}{2} - V_x\right)\right\} \\ &= I_1 + I_2. \end{aligned}$$

Furthermore, assuming that $k_4 = k_5$, I_4 and I_5 are given by

$$\begin{aligned} I_4 &= I_{bec} \exp\left\{\frac{k_2}{nU_T} \left(V_{in1} - \frac{V_{dd}}{2}\right)\right\} \\ &\quad \cdot \exp\left\{\frac{k_4}{nU_T} \left(V_x - \frac{V_{dd}}{2}\right)\right\} \\ &= \frac{(I_{bec})^2}{I_3} \exp\left\{\frac{k_2}{nU_T} \left(V_{in1} - \frac{V_{dd}}{2}\right)\right\} \\ I_5 &= I_{bec} \exp\left\{\frac{k_2}{nU_T} \left(V_{in2} - \frac{V_{dd}}{2}\right)\right\} \\ &\quad \cdot \exp\left\{\frac{k_4}{nU_T} \left(V_x - \frac{V_{dd}}{2}\right)\right\} \\ &= \frac{(I_{bec})^2}{I_3} \exp\left\{\frac{k_2}{nU_T} \left(V_{in2} - \frac{V_{dd}}{2}\right)\right\}. \end{aligned}$$

Finally, assuming that $I_6 = I_4$, the output current becomes

$$\begin{aligned} I_{out} &= I_6 - I_5 \\ &= I_{bec} \exp\left\{\frac{k_3}{nU_T} \left(\frac{V_{dd}}{2} - V_b\right)\right\} \left(\frac{I_1 - I_2}{I_1 + I_2}\right) \\ &= I_b \tanh\left\{\frac{k_1}{2nU_T} (V_{in1} - V_{in2})\right\} \end{aligned}$$

Fig. 4. ULV floating-gate tanh-shaped transconductance amplifier.

Fig. 5. Measured output current of the tanh-shaped transconductance amplifier with $V_{dd} = 0.8$ V.

where

$$I_b = I_{bec} \exp\left\{\frac{k_3}{nU_T} \left(\frac{V_{dd}}{2} - V_b\right)\right\}.$$

Measured output current of the tanh-shaped transconductance amplifier is shown in Fig. 5.

Traditionally, the main disadvantage of using operational transconductance amplifiers (OTAs) has been the highly restricted differential input voltage swing required to maintain linearity of the output current. Capacitive division factors have been exploited in order to make a wider linear range [7]. By scaling the input capacitive division factors of the transconductance amplifiers, the linear range of the output current with respect to differential input voltage may be increased. It can be shown that by scaling down the input capacitive division factor, we obtain an increased linear range. The consequence of widening the linear range of the output current is a more constant transconductance for the device, which in turn leads to a better performance with respect to harmonic distortion [6]. A sinh-shaped OTA is more linear than a tanh-shaped OTA [7].

Fig. 6. Floating-gate analog inverter circuit with corresponding symbol.

IV. A FOUR-TRANSISTOR SYMMETRIC RAIL-TO-RAIL ULTRA-LOW-VOLTAGE TRANSCONDUCTANCE AMPLIFIER

A. The Floating-Gate Analog Inverter

The currents in Fig. 6 can be expressed as

$$\begin{aligned} I_n &= I_{bec} \exp\left\{\frac{1}{nU_t} \left(V_i - \frac{V_{dd}}{2}\right) k_i\right\} \\ &\quad \cdot \exp\left\{\frac{1}{nU_t} \left(V_{out} - \frac{V_{dd}}{2}\right) k_r\right\} \\ I_p &= I_{bec} \exp\left\{\frac{1}{nU_t} \left(\frac{V_{dd}}{2} - V_i\right) k_i\right\} \\ &\quad \cdot \exp\left\{\frac{1}{nU_t} \left(\frac{V_{dd}}{2} - V_{out}\right) k_r\right\}. \end{aligned}$$

$I_n = I_p$ and $k_i = k_r$ give $V_{out} = V_{in}^* \equiv V_{dd} - V_{in}$ and $I_n = I_p = I_{bec}$. The output gain is controlled by the capacitive division factors k_i and k_r (C_i and C_r). By using a slightly smaller k_r compared to k_i , we can compensate for the output conductance measured characteristics of the analog inverter shown in Fig. 7.

B. The FGUMOS ULV Output Stage

A “digital” double input inverter, as shown in Fig. 8, can be used as a ULV output stage. The output current of the inverter in Fig. 8 is given by

$$\begin{aligned} I_{out} &= I_p - I_n \\ &= I_{bec} \exp\left\{\frac{1}{nU_t} \left(V_b - \frac{V_{dd}}{2}\right) k_b\right\} \\ &\quad \cdot \left[\exp\left\{\frac{1}{nU_t} \left(\frac{V_{dd}}{2} - V_{in1}\right) k_{i1}\right\} \right. \\ &\quad \cdot \exp\left\{\frac{1}{nU_t} \left(\frac{V_{dd}}{2} - V_{in2}\right) k_{i2}\right\} \\ &\quad \left. - \exp\left\{\frac{1}{nU_t} \left(V_{in1} - \frac{V_{dd}}{2}\right) k_{i1}\right\} \right. \\ &\quad \left. \cdot \exp\left\{\frac{1}{nU_t} \left(V_{in2} - \frac{V_{dd}}{2}\right) k_{i2}\right\} \right]. \end{aligned}$$

$k_{i1} = k_{i2} = k_i$ gives $I_{out} = -2I_{bec} \exp\{(1/nU_t)(V_b - V_{dd}/2)k_b\} \sinh\{(1/nU_t)(V_{in1} + V_{in2} - V_{dd})k_i\}$. In order to

Fig. 7. Measured analog inverting amplifier characteristics for equilibrium currents ranging from 0.5 nA to 2 μ A.

get a symmetric differential output current, we substitute V_{in} with $V_{in}^* = V_{dd} - V_{in}$. Although the bias input can be used to set the appropriate current level, it will decrease the gain due to the reduced input capacitive division factors, that is, $k_{o_{max}} \leq 1/2 - k_b$. If a wide linear range is required for some application, we can increase the linear range by applying a small input capacitive factor k_{i1} and k_{i2} by using the bias input and/or smaller input capacitors C_{i1} and C_{i2} .

C. Symmetric Differential Rail-to-Rail Ultra-Low-Voltage Amplifier

By using an analog inverter and a double-input inverter, we obtain two slightly different four-transistor transconductance amplifiers, shown in Fig. 9(a) and (b).

The ultra-low-voltage amplifier shown in Fig. 10 has an output current, which is given by

$$I_{out} = 2I_b \sinh \left\{ \frac{1}{nU_t} (V_{dd} - V_x - V_{in2}) k_o \right\} \quad (1)$$

where $I_b = I_{bec} \exp\{(1/nU_t)(V_b - V_{dd}/2)k_b\}$. Substituting $V_x = V_{dd} - V_{in1}$ into (1) leads to

$$I_{out} = 2I_b \sinh \left\{ \frac{1}{nU_t} (V_{in1} - V_{in2}) k_o \right\}.$$

SpectreS [8] simulations of the ULV amplifier with capacitor values $C_i = 11$ fF, $C_r = 10$ fF, $C_o = 12$ fF (pMOS), $C_o = 8$ fF (nMOS), and $C_b = 6$ fF are shown in Fig. 11.

V. SYMMETRIC ULV AMPLIFIER WITH TUNABLE GAIN AND LINEARITY

A. The Output Stage

The current out of the floating-gate ULV OTA output stage shown in Fig. 12 is

$$I_{out} = I_p - I_n$$

Fig. 8. (a) Double-input inverter. (b) Double-input inverter with bias input.

Fig. 9. Floating-gate amplifiers with and without bias input.

Fig. 10. Symmetric ULV floating-gate amplifier.

$$\begin{aligned} &= I_b \left[\exp \left\{ \frac{k_i}{nU_t} \left(\frac{V_{dd}}{2} - V_{in} \right) \right\} \right. \\ &\quad \left. - \exp \left\{ \frac{k_i}{nU_t} \left(V_{in} - \frac{V_{dd}}{2} \right) \right\} \right] \\ &= 2I_b \sinh \left\{ \frac{k_i}{nU_t} \left(\frac{V_{dd}}{2} - V_{in} \right) \right\} \end{aligned}$$

where $I_b = I_{bec} \exp\{(k_b/nU_t)(V_b - V_{dd}/2)\}$ and k_i is the capacitive division factor for input V_{in} .

The output stage resembles a digital FGVMOS inverter [9]. We need to connect a differential input stage to the OTA output stage in order to obtain a differential ULV OTA. The analog additive inverter together with the analog inverter can be used to provide a differential input stage.

Fig. 11. Simulated floating-gate amplifier characteristics.

B. The Floating-Gate Additive Analog Inverter

The analog additive inverter with a differential bias input can be used to provide a differential input stage. The currents in Fig. 13 can be expressed as, assuming $V_1 = V_{in1}$ and $V_2 = V_{in2}$

$$\begin{aligned} I_{pi} &= I_{b1} \exp\left\{\frac{k_i}{nU_t} (V_{dd} - V_1 - V_2)\right\} \\ I_{ni} &= I_{b1} \exp\left\{\frac{k_i}{nU_t} (V_1 + V_2 - V_{dd})\right\} \\ I_{pr} &= I_{b2} \exp\left\{\frac{k_r}{nU_t} (V_{dd}/2 - V_{out})\right\} \\ I_{nr} &= I_{b2} \exp\left\{\frac{k_r}{nU_t} (V_{out} - V_{dd}/2)\right\} \end{aligned}$$

where

$$\begin{aligned} I_{b1} &= I_{bec} \exp\left\{\frac{k_b}{nU_t} (V_{b1} - V_{dd}/2)\right\} \\ I_{b2} &= I_{bec} \exp\left\{\frac{k_b}{nU_t} (V_{b2} - V_{dd}/2)\right\}. \end{aligned}$$

We have that $I_{pi} + I_{pr} = I_{ni} + I_{nr}$, $V_{b1} = V_{b2} = V_{dd}/2$ and $k_r = 2k_i$ gives $V_{out} = \{(V_1 + V_2)/2\}^* \equiv V_{dd} - (V_1 + V_2)/2$ and $I_n = I_p = I_{bec}$. The output gain is controlled by the capacitive division factors k_i and k_r (C_i and C_r). By using a

Fig. 12. The floating-gate ULV OTA output stage.

Fig. 13. Floating-gate additive analog inverter.

Fig. 14. Measurements of the additive analog inverter.

slightly smaller k_r compared to k_i , we can compensate for the output conductance. The input capacitive division factor can be

Fig. 15. Measured gain of the inverting amplifier for equilibrium currents of 4–40 nA.

Fig. 16. Measured inverting amplifier characteristics for equilibrium currents of 4–40 nA.

exploited to increase the linearity and reduce the gain. If $k_r = 4k_i$, then $V_{out} = \{(V_1 + V_2)/4\}^*$.

The differential bias input provides a dynamic Gm/linearity control. Measured output characteristics of the additive analog inverter are shown in Fig. 14 for different equilibrium currents ranging from 1 to 100 nA. The gain is independent of the equilibrium current for current levels in weak inversion, as shown in Fig. 15. The output characteristics of the additive analog inverter with tunable gain are shown in Fig. 16. If $V_{b1} \ll V_{b2}$, the output can be approximated by the $\sinh$ function, that is, $V_{out} \approx V_{dd}/2(1 - \sinh\{K(V_1 + V_2 - V_{dd})\})$, where K is inversely proportional to $V_{b2} - V_{b1}$. Furthermore, if $V_{b1} \gg V_{b2}$, the output can be approximated by the $\tanh$ function, that is, $V_{out} \approx V_{dd}/2(1 - \tanh\{K(V_1 + V_2 - V_{dd})\})$, where K is inversely proportional to $V_{b1} - V_{b2}$. The output voltage may be expressed as $V_{out} = F(V_{dd} - (V_1 + V_2)/2)$, where F can be a $\sinh$, $\tanh$, or linear function depending on the bias inputs. The gain range for equilibrium current equal to 10 nA is shown in Fig. 17. By increasing k_b , and implicitly decreasing k_i , we can increase the gain range further.

Fig. 17. Measured gain of the inverting amplifier as a function of bias voltage.

Fig. 18. Floating-gate ULV amplifier with variable gain.

If we connect the additive analog inverter to the OTA output stage, assuming that $k_r = 2k_i$, the output current becomes

$$I_{out} = 2I_b \sinh\left\{\frac{k_i}{nU_t}(V_{dd}/2 - F(V_{dd} - (V_1 + V_2)/2))\right\}.$$

If we apply $V_1 = V_2^*$, we obtain

$$I_{out} = 2I_b \sinh\left\{\frac{k_i}{nU_t}(V_{dd}/2 - F(V_{dd}/2 - V_2 - V_1)/2))\right\}.$$

C. Floating-Gate ULV Variable Transconductance OTA

The ULV variable Gm OTA is shown in Fig. 18. The analog inverter, additive analog inverter, and “digital” inverter symbols can be used to simplify analog floating-gate design. Note that the analog inverter and the additive analog inverter constitute a differential analog inverter. We are using digital and analog “gates,” and the individual gates may be designed in different ways.

An example of a transistor-level design of the ULV variable Gm OTA is shown in Fig. 19. The amplifier has three internal nodes. Preliminary voltage-mode measurements of the ULV OTA are shown in Fig. 20, showing both the internal node V_x and the output. With a supply voltage of 0.8 V, a rail-to-rail operation is demonstrated with settings giving high voltage gain. The gain of the amplifier can be increased by using larger input capacitors and by increasing the transistor length in the output stage. Measured output currents and normalized transconductance of the OTA for different biasing conditions are shown in Figs. 21 and 22, respectively. By increasing $V_{b1} - V_{b2}$, we increase the gain in the analog additive inverter

Fig. 19. Floating-gate ULV amplifier with variable gain.

Fig. 20. Preliminary measurements of the ULV OTA.

Fig. 21. Measurement of the ULV OTA for several values of bias inputs.

and implicitly increase the transconductance of the amplifier. The increase in $V_{b1} - V_{b2}$ shapes the output of the analog additive inverter more toward a tanh-shaped transfer function. The result of this shaping is that the output current may be modeled as a $\sinh(\tanh(V_{in}))$ function, and thus the linear range is increased as shown in Fig. 22.

Finally, the simulated magnitude and phase of the ULV variable Gm OTA are shown in Fig. 23. Since we did not add output

Fig. 22. Measurement of the ULV OTA for several values of bias inputs.

Fig. 23. SpectreS ac simulation showing the magnitude and phase of the OTA.

drivers for our circuits, no frequency measurements are provided.

VI. CONCLUSION

Ultra-low-voltage floating-gate sinh-shaped and tanh-shaped transconductance amplifiers are presented. We have introduced the symmetric ULV analog inverter, the symmetric double input inverter, and the symmetric additive (double input) analog inverter with tunable gain. We use these “gates” in ULV rail-to-rail symmetric differential transconductance amplifiers. Two examples of symmetric ULV floating-gate transconductance amplifiers are presented. Measured data are provided.

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